PACKET CONFIGURING METHOD AND PACKET RECEIVER

BACKGROUND OF THE INVENTION

The present invention relates to a packet configuring method and a packet receiver. Particularly, the present invention relates to a packet configuring method and a packet receiver, each for configuring a packet that contains training sequences in an asynchronous packet communication mode.

Fig. 7 is a diagram illustrating a down-link control channel frame used for the conventional digital automobile telephone, described ETSI/GSM, "Recommendation GSM 05.02 Multiplexing and Multiple Access on the Radio Path", version 3.3.0, 15, April, 1989. Fig. 7 shows an example of a 10-channel configuration being the head of a frame. This frame is formed of a frequency connection channel (FCCH) 1000, a synchronization channel (SCH) 1001 and a broadcast channel (BCCH) 1002. The slot forming SCH 1001 or BCCH 1002 is formed of the training portion 1011 and the data portions 1010 sandwiched by the training portion 1011. The frequency connection channel FCCH 1000 is formed of a sine wave signal with a single frequency.

The mobile station that receives the control channel operates as follows: First, the mobile station receives FCCH 1000 and then corrects a variation in frequency

(frequency offset) between a transmitter and a receiver. Then, the mobile station demodulates the synchronization channel SCH 1001 and the broadcast channel BCCH 1002.

SCH 1001 and BCCH 1002 are demodulated as follows: First, a channel impulse response is obtained using the training portion 1011. SCH 1001 and BCCH 1002 are demodulated by setting the reception parameter for the receiver based on the resultant channel impulse response. That is, the training portion 1011 is used for the initializing of the receiver.

According to the conventional art described above, frequency offset compensation and channel impulse response estimation necessary for signal reception are differently obtained.

In the automobile telephone system where communications are not always established through a base station but either communications via the base station or direct communications between terminals are established, for example, in local area networks (LANs), there is the possibility that different signal transmission sources are used for respective packets. This requires the receiver to execute frequency offset compensation and channel impulse response estimation every packet reception. In such a case, it may be considered, as shown in Fig. 8, that both the sequences 1020 for frequency offset estimation and the

sequences 1021 for channel impulse response estimation are contained in the training sequences.

There is the method where the receiver monitors, for example, the reception power and the packet transmission to detect a transmitted packet in an asynchronous packet transmission and detects when the reception power exceeds a predetermined threshold value. In this case, the head of a packet cannot be already received accurately due to influences of noises or radio transmission path. Hence, this method has the disadvantage in that the boundary between the sequence for frequency offset estimation and the sequence for channel impulse response estimation may not be recognized.

Moreover, the method has the disadvantage in that the length of a training sequence is prolonged using the sequence for frequency offset estimation and the sequence for channel impulse response estimation, whereby the transmission efficiency is degraded.

SUMMARY OF THE INVENTION

The present invention is made to solve the above-mentioned problems.

Moreover, the objective of the invention is to provide a packet configuration method that correctly estimates an estimate frequency offset and a channel impulse and then demodulates a received packet even when a transmitted

packet is erroneously detected in timing in the communication mode where packets are asynchronously transmitted.

Another objective of the present invention is to provide a packet receiver that correctly estimates an estimate frequency offset and a channel impulse response and then demodulates a received packet even when a transmitted packet is erroneously detected in timing in the communication mode where packets are asynchronously transmitted.

The objective of the present invention is achieved by a method configuring packets, the packets each having a training portion and a data portion to set a receiver, comprising the step of forming the training portion by serially connecting K sequences (where K is an integer of 2 or more), each of the K sequences being formed of N symbols (where N is an integer of 2 or more).

According to the present invention, a packet receiver receives packets each which is formed of a training portion and a data portion to initialize of the receiver. The packet receiver comprises frequency-offset estimation means for estimating a frequency offset based on a received packet, frequency-offset compensation means for compensating a frequency offset contained in the received packet based on the frequency offset estimation value, and

channel impulse response estimation means for estimating an impulse response of a channel based on an output of which the frequency offset is compensated.

That is, the same sequences, each formed of N symbols, are repeatedly used in a communication mode where packets are asynchronously transmitted. Thus, the frequency offset can be estimated by detecting the phase difference between a signal received before NT and a currently-received signal.

In a packet formed of a training portion and a data portion to initialize a packet receiver according to the present configuring method, the training portion has K sequences chained, each being formed of N symbols, to estimate a frequency offset and a channel impulse response. The auto-correlation function of a sequence formed of N symbols is in an impulse state.

Moreover, the packet receiver comprises a frequency offset estimation circuit for estimating a frequency offset of a received signal and then outputting a frequency offset estimation value, a frequency offset compensation circuit for receiving the frequency offset estimation value and the received signal and compensating a frequency offset contained in the received signal based on a frequency offset estimation value, and a channel impulse response estimation circuit for receiving an

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output from the frequency offset compensation circuit, estimating a channel impulse response, and then outputting the channel impulse response estimation value after inputting a frequency offset estimation completion pulse.

The frequency offset estimation means comprises a delay circuit for receiving a received signal and delaying the received packet by a transmission period of time corresponding to N-symbols; a phase difference detection circuit for detecting a phase difference between an output of the delay circuit and the received packet; an integrator for integrating a detection output of the phase difference detection circuit over a transmission period of time of a sequence of M symbols; and a divider circuit for dividing an output of the integrator by a product of N and M.

According to the present invention, the sequence for estimation of a frequency offset and the sequence for estimation an impulse response are not separated from each other and are defined as repetition of the same sequences. The phase difference between the i-th symbols in each sequence is detected using this configuration, so that the frequency offset can be estimated. This feature allows the frequency offset to be estimated correctly even when a packet is detected with an erroneous timing.

Furthermore, where the auto-correlation function in an

impulse state is used as the same sequence, a channel impulse response can be estimated by the simple operation that the receiver examines the correlation between the sequence and a received training sequence.

According to the present invention, since the frequency offset estimation and the channel impulse response estimation can be performed using the same sequences, the frequency offset estimation sequence and the channel impulse response estimation sequence are equivalently overlapped. This configuration can reduce the length of the training sequence.

BRIEF DESCRIPTION OF THE DRAWINGS

This and other objects, features, and advantages of the present invention will become more apparent upon a reading of the following detailed description and drawings, in which:

Fig. 1 is a format diagram illustrating a packet having a training sequence which is configured according to the training sequence configuration method of an embodiment of the present invention;

Fig. 2 is a diagram illustrating an auto-correlation function of a sequence of 32 symbols applicable for the training sequence configuring method of the present invention;

Fig. 3 is a diagram illustrating a principle of

obtaining an auto-correlation function;

Fig. 4 is a diagram explaining a principle of estimating a frequency offset from the training sequence of Fig. 1;

Fig. 5 is a systematic diagram illustrating a receiver that receives packets having the training sequence of Fig. 1;

Fig. 6 is a systematic diagram illustrating a frequency offset estimation circuit that estimates a frequency offset based on the training sequence of Fig. 1;

Fig. 7 is a diagram illustrating a format of a conventional frame; and

Fig. 8 is a diagram illustrating the format of a packet to estimate a frequency offset and a channel impulse response with a different sequence.

DESCRIPTION OF THE EMBODIMENTS

An embodiment of the present invention will be described below with reference to the attached drawings. In the drawings, like numerals represent the same elements.

Fig. 1 is a diagram illustrating a packet format configured according to the packet configuration method of the present invention. Referring to Fig. 1, a packet 10 is formed of a training portion 101 and a data portion 102. The training portion 101 is formed of sequences 100-1 to 100-K each formed of the same N symbols. That is, the training portion is formed of K sequences serially

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connected, each being formed of N symbols.

As an N symbol sequence, for example, in the case of N = 32, the following sequence 1 formed of two symbols including the symbol "1" and the symbol "0" can be used.

Sequence 1: 11111100110101001000001100101000

The sequence 1 is merely represented as an example. Other sequences can be used by arbitrarily combining the symbols "1" and "0".

In the sequence 1, when the value corresponding to the symbol "1" corresponds to +1 and 0 and the value corresponding to the symbol "0" corresponds to -1 and 0, the auto-correlation function is plotted as shown in Fig. 2.

In Fig. 2, the x-axis represents symbol differences and the y-axis represents auto-correlation values. When the auto-correlation of the sequence 1 is obtained as shown in Fig. 3, it is assumed that the x-axis has a symbol difference of 0 in the case where the sequence 1 is completely in a synchronized state. The symbol numbers where the sequence 1 is shifted to the right represent positive symbol differences. The symbol numbers where the sequence 1 is shifted to the left represent negative symbol differences.

As shown in Fig. 2, the auto-correlation function of the sequence 1 becomes an impulse over a symbol difference

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value of -13 to +13. By using such a nature and the correlation circuit shown in Fig. 7 disclosed, for example, in Japanese Patent publication No. 2600970 (or USP No. 5,127,025), the channel impulse response can be estimated over the time period corresponding to 13 symbols. This operation allows the received signal and the N-symbol sequence to be correlated. Even when the packet is detected with an erroneous timing, an error of packet detection timing can be absorbed by detecting a peak correlation value.

The frequency offset can be estimated as follows: That is, a transmission symbol is overlapped with another transmission symbol in the channel with time dispersion characteristics, so that a distortion called a inter-symbol interference occurs. Where the channel impulse response on the channel is regarded as constant, that distortion is uniquely decided by the channel impulse response and transmission symbol sequence. In this case, when the same sequences transmitted in series is received, the receiver receives signals subjected to the same distortion.

If there is a frequency offset of ω between the receiver and the transmitter, the phase difference $\Delta\theta$ between the i-th symbols ($i = 1, 2, \ldots, N$) respectively transmitted to the j-th symbol sequence and (j+1)-th

symbol sequence, as shown in Fig. 4, is equal to ω x NT, where T is a continuous time of 1 symbol and is previously determined by a transmission rate.

As described above, the receiver can detect the phase difference between a signal received prior to the time NT and a currently received signal, using as a training sequence a sequence where the same sequences of N symbol are repeatedly chained, so that the frequency ω can be estimated. That is, the frequency offset is estimated based on a phase difference between two neighboring sequences. Since this operation can executed to any symbol within each N symbol sequence, it is not adversely affected with the detection timing of packet reception.

The configuration of the receiver that performs the above-mentioned operation is shown in Fig. 5. Referring to Fig. 5, the receiver consists of an input terminal 110, a power detection circuit 111, a sampler 112, a frequency offset estimation circuit 113, a frequency offset compensation circuit 114, a channel impulse response estimation circuit 115, an equalizer 116, and an output terminal 117.

A reception signal is input to the power detection circuit 111 and the sampler 112 via the input terminal 110. The power detection circuit 111 detects the power of the received signal. The power detection circuit 111 judges

that a packet has been transmitted when the detected power exceeds a predetermined threshold value, and then outputs a packet detection pulse.

The sampler 112 samples the received signal in response to a packet detection pulse. The sampled reception signal is input to the frequency offset estimation circuit 113 and the frequency offset compensation circuit 114.

After the inputting of the packet detection pulse, the frequency offset estimation circuit 113 estimates a frequency offset based on a sampled reception signal and then outputs a frequency offset estimation value. The frequency offset estimation circuit 113 can be configured, for example, as shown in Fig. 6.

Referring to Fig. 6, the frequency offset estimation circuit 113 consists of an input terminal 120, a delay circuit 121 for delaying an input signal, a phase difference detection circuit 122 for detecting a phase difference between a delayed signal and an input signal, an integrator 123 for integrating a detected phase difference, a memory 125, a divider 124 for dividing the output from the integrator 123 by an output value from the memory, and an output terminal 126.

In such a configuration, a sampled reception signal, or an output signal of the sampler 112, is input to the input terminal 120. Where a 32 symbol sequence 1 is used as a

training sequence, the delay circuit 121 delays it by the time period corresponding to 32 symbols being the transfer time of the sequence 1. Since a received signal with a time difference corresponding to 32 symbols is formed of the totally same symbols, the signal shifted by the phase difference is obtained based on the frequency difference when a frequency offset occurs.

The phase difference detection circuit 122 receives the output of the delay circuit 122 and the sampled reception signal input to the input terminal 120 to detect the phase difference between the input signals. In other words, the output of the phase difference detection circuit 122 is equal to a variation in phase ($\Delta\theta$) of the N symbol time produced by the frequency offset, as shown in Fig. 4.

The integrator 123 integrates M outputs from the phase difference detection circuit 122, thus reducing adverse effects due to noises. The output of the integrator 123 becomes a variation in phase corresponding to M x N symbols caused by the frequency offset.

The divider circuit 124 divides the value integrated by the integrator 123 by the constant M x N output from the memory 125. The divider circuit 124 also converts the integrated value of the integrator 123 into the phase rotating within one symbol period by the frequency offset and then outputs the converted value to the output

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terminal 126.

The frequency offset compensation circuit 114 compensates the frequency offset by rotating the phase of a reception signal sampled based on an input frequency offset estimation value in the frequency-offset compensation direction. The frequency-offset compensated signal is input to the channel impulse response estimation circuit 115 and the equalizer 116.

Where the sequence in which the sequence is repeatedly obtained is used as a training sequence, the channel impulse response estimation circuit 115 can be realized using the correlation circuit as shown in Fig. 7, for example, disclosed Japanese Patent publication No. 2600970 (or USP No. 5,127,025). The channel impulse response estimation value is output to the equalizer 116. The channel impulse response estimation value is output after the pulse representing that the frequency offset estimation of the frequency offset estimation circuit 113 has been completed is output.

The equalizer 116 demodulates the sampled reception signal based on the channel impulse response estimation value output from the channel impulse response estimation circuit 115. Japanese patent publication No. 2600970 (or USP No. 5,127,025) discloses the maximum likelihood sequence estimator that configures a replica of a received

signal based on a channel impulse response estimation value and all possible transmission symbol sequences and then outputs as a demodulation result a sequence creating a replica most similar to an actual reception signal, in Figs. 8 to 12. This likelihood sequence estimator can be used as the equalizer 116.

As described above, the present invention can correctly estimate a frequency offset and a channel impulse response even when a transmitted packet is detected with an erroneous timing in an asynchronous packet communication mode, thus demodulating the packet.

According to the present invention, a training sequence is formed by serially connecting sequences, each being formed of the same N symbols. Even in the channel where a inter-symbol interference occurs, the reception signal shifted by the N symbol time period corresponds to a signal shifted by a different phase caused by the frequency offset between the transmitter and the receiver, using the training sequence. Hence, the present invention has the advantage in that the frequency offset can be estimated even when the timing of detecting the head of a packet is erroneous.

The entire disclosure of Japanese Application No. 10-192219 filed July 8, 1998 including specification, claims, drawing and summary are incorporated herein by reference

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in its entirely.